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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,151	09/22/2003	Vishnu K. Agarwal	M4065.0195/P195-B	5782

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EXAMINER	
PHAM, HOAI V	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/665,151	AGARWAL ET AL.	
	Examiner	Art Unit	
	Hoai v. Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2005*.

2a)☒ This action is **FINAL**. 2b) This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,23,28,39,44 and 77-85* is/are pending in the application.

4a) Of the above claim(s) *4,7,12,14 and 15* is/are withdrawn from consideration.

5)☒ Claim(s) *23,28,39,44,77,84 and 85* is/are allowed.

6)☒ Claim(s) *1-3,5,6,8-11 and 78-83* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 5, 6, 9-11, and 78-83 are rejected under 35 U.S.C. 102(e) as being anticipated by Anand et al. [U.S. Pat. 6,307,265].

With respect to claim 1, Anand et al. (fig. 7, col. 18) discloses a monolithic semiconductor device comprising:

a semiconductor substrate (21);

a plurality of microstructures (28a, 28b) formed over the substrate (21); and

a brace (29) transversely extending between lateral sides of at least two of the microstructures (28a, 28b); and

a vertical space (31) between said brace and said semiconductor substrate.

With respect to claim 2, Anand et al. discloses that the brace (29) interconnects substantially all of the microstructures (see fig. 7).

With respect to claim 3, Anand et al. discloses that the brace (29) is located substantially near upper ends of the microstructures (28a, 28b) (see fig. 7).

With respect to claim 5, Anand et al. discloses that the brace (29) comprises a microbridge structure extending above the substrate (21) and between two or more of the microstructures (28a, 28b) (see fig. 7).

With respect to claim 6, Anand et al. discloses that the microstructures (28a, 28b) each comprise a conductor material (see col. 18, lines 35-47) portion standing upright over the substrate (21), and wherein the brace (29) interconnects the conductor material portion of two or more of the microstructures (28a, 28b) (see fig. 7).

With respect to claim 9, Anand et al. discloses that the brace (29) comprises a dielectric material (see col. 18, lines 49-51).

With respect to claim 10, Anand et al. discloses that a dielectric (25) between the substrate (21) and the brace (29), wherein the brace is vertically spaced from the dielectric layer (see fig. 7).

With respect to claim 11, Anand et al. discloses that the wherein the microstructures (28a, 28b) comprise conductive material (see col. 18, lines 35-47) and the brace (29) comprises a dielectric (see col. 18, lines 49-51).

With respect to claim 78, Anand et al. (fig. 7, col. 18) discloses a support structure on a semiconductor device comprising:

a plurality of braces (29) transversely extending between lateral sides of microstructures (27a, 28a, 27b, 28b) formed over a semiconductor substrate (21), wherein said plurality of braces (29) comprise a support structure for said plurality of microstructures (27a, 28a, 27b, 28b); and a vertical space (31) between the plurality of braces (29) and the semiconductor substrate (21).

With respect to claim 79, Anand et al. (fig. 7, col. 18) discloses a brace for a semiconductor device comprising:

at least one brace (29) transversely extending between lateral sides of at least two microstructures (27a, 28a, 27b, 28b) on a semiconductor substrate (21), wherein said at least two microstructures (27a, 28a, 27b, 28b) are supported only by said at least one brace, wherein said at least one brace comprises one material layer.

With respect to claim 80, Anand et al. (fig. 7, col. 18) discloses an in-process semiconductor device comprising:

a semiconductor substrate (21);

at least two microstructures (27a, 28a, 27b, 28b) formed over the substrate (21); and

at least one brace (29) transversely extending between lateral sides of at least two microstructures (27a, 28a, 27b, 28b), wherein said at least two microstructures

(27a, 28a, 27b, 28b) are supported only by said at least one brace (29), and wherein said at least one brace comprises a single material layer.

With respect to claim 81, Anand et al. (fig. 7, col. 18) discloses a semiconductor support structure, comprising:

a semiconductor substrate (21);

a plurality of microstructures (27a, 28a, 27b, 28b) formed over the substrate (21); and

at least one brace (29) transversely extending between lateral sides of at least two of said plurality of microstructures (27a, 28a, 27b, 28b), wherein the brace (29) comprises a support structure (29), and wherein there is a vertical space (31) between the support structure (29) and the semiconductor substrate (21)..

With respect to claim 82, Anand et al. discloses that the at least one brace comprises a plurality of braces (29) (see fig. 7).

With respect to claim 83, Anand et al. discloses that the plurality of braces (29) form a lattice support structure (see fig. 7).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anand et al. [U.S. Pat. 6,307,265].

Anand et al. substantially discloses all the limitation as claimed above except that the microstructures comprise generally solid cylindrical shapes. It would have been an obvious matter of design choice to form microstructures comprising generally solid cylindrical shapes as applicant claimed, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1995).

Allowable Subject Matter

6. Claims 23, 28, 39, 44, 77, and 84-85 are allowed.

7. Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments with respect to claims 1-3, 5-6, 8-11, and 78-83 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

10. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HOAI PHAM
PRIMARY EXAMINER